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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,943	12/18/2001	Hamid Reza Rategh	M-12365 US	6679

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EXAMINER	
NGUYEN, LINH V	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/024,943	Applicant(s) RATEGH ET AL.	
	Examiner Linh V Nguyen	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 2, 6 –12, and 14 - 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujioka et al. U.S. patent No. US 6492872.

Regarding to claim 1, Fig. 9 Fujioka et al. disclose a method for improving an input match in a circuit comprising: operating a cascade having an input signal port (Gate of Q1) with an input signal impedance (MC1) and further having a stage gain controlled by a level setting gain control voltage (Vapc); and operating an impedance compensating circuit for changing a compensating impedance presented at the input

signal port (22), wherein the impedance compensating circuit is controlled by the level setting gain control voltage (Vapc) and wherein the impedance compensating circuit is operable to counteract changes in the input signal impedance correlated with changes in the stage gain(Fig. 14, 15).

Regarding to claim 2, the method of claim 1 wherein: the impedance compensating circuit is connected in parallel with the input signal port (Fig. 11).

Regarding to claim 6 the method of claim 1 wherein: the cascade is implemented using metal-oxide semiconductor transistors formed as an integrated circuit (Fig. 11).

Regarding to claim 7. The method of claim 1 wherein: the cascade is implemented using devices selected from a list consisting of metal-oxide semiconductor transistors, silicon bipolar transistors and germanium transistors (Fig. 11).

Regarding to claims 8, and 16, Fig. 11 Fujioka et al. disclose a circuit for processing a signal comprising: a cascade having a first transistor (Q1) connected in a configuration selected from a group consisting of a common gate configuration and a common base configuration and a second transistor (24) connected in a configuration selected from a group consisting of a common source configuration, a common drain configuration, a common emitter configuration and a common collector configuration; a gain controller (22) operable to adjust a gain of the cascade in response to a control signal (22); and an impedance controller (22) operable to adjust an input impedance (MC1) of the cascade with a loading impedance (28) in response to the control signal (Vapc); whereby the circuit operates with input impedance compensation.

Regarding to claim 9, the circuit of claim 8 wherein the circuit is an amplifier (Fig. 11).

Regarding to claims 10, and 17, the circuit of claim 8 wherein the circuit is an amplifier that operates at a narrow band of frequencies in the microwave region (Col. 8 line 44).

Regarding to claims 11 and 18, the circuit of claim 8 wherein the circuit is implemented as a single integrated circuit (Col. 8 line 44).

Regarding to claims 12 and 19, the circuit of claim 8 wherein the circuit is implemented using metal-oxide semiconductor technologies (Fig. 11).

Regarding to claim 14, the circuit of claim 8 wherein the impedance controller comprises an inverter (Fig. 2, inverting input of 19).

Regarding to claim 15. The circuit of claim 8 wherein the gain controller outputs a DC bias voltage that is applied to a control terminal of the first transistor (Figs. 11, 14, 15).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujioka et al.

Fig. 11, Fujioka et al. as applied to claim 1 disclose every aspect of applicant's claimed invention except for the compensation circuit is connected in series or series-parallel with the input signal port.

At the time the invention was made, it would have been to a person of ordinary skill in the art to have the compensation circuit (22) of Fujioka et al. connecting series, or series parallel to the input port since in the specification and figures of applicant have not disclose the series, or series-parallel connection and provides any advantage, which is used for a particular purpose, or solves a stated problems. One of ordinary skill in the art would have expected applicant's invention to perform equally well with Fig. 11 of Fujioka et al. because it has indicated equivalent by applicant's invention, 2, 3 and 4.

5. Claims 5, 13, and 20, rejected under 35 U.S.C. 103(a) as being unpatentable over Fujioka et al. as applied to claims 1, 8 and 16 above, and in view of Applicant's Admitted Prior Art (AAPA).

Fig. 11, Fujioka et al. as applied to claims 1, 8, and 16 above, disclose every aspect of applicant's claimed invention, except for not explicitly disclose the circuit is implemented using Gallium Arsenide technologies, however Gallium Arsenide technologies is a well know art in amplifier circuit as have indicated by AAPA (page 2, lines 5 – 7). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made have the amplifier circuit of Fujioka implemented using Gallium Arsenide as have indicated by AAPA.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

June 10, 2003

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800